EVOLUTION AND APPLICATIONS OF SYSTEM ON A CHIP SPACEWIRE COMPONENTS FOR SPACEBORNE MISSIONS*

Session: Components 2

Long Paper

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ABSTRACT

As reported at the first SpaceWire International Conference in 2007, BAE Systems in conjunction with NASA has created and space qualified a radiation hardened SpaceWire system on a chip ASIC containing a four port SpaceWire router, embedded microcontroller and memory, built-in memory, discrete, test and dual PCI interfaces. This ASIC has been inserted into a number of missions, including both the single board computer and the Mini-RF payload for the Lunar Reconnaissance Orbiter (LRO) NASA Mission planned for launch in early 2009. This versatile ASIC also supports creating routers scalable beyond its four ports. The SpaceWire core has been updated by NASA and was integrated with other ASIC functions into BAE Systems' latest RAD750™ bridge ASIC, the Golden Gate, shrinking the number of ASICs required for a Processor with SpaceWire by two-thirds.

This paper will describe the BAE Systems' SpaceWire ASIC's use within and between the Mini-RF system and the LRO Spacecraft as well as details about the board containing the ASIC and software supporting it mission. This paper will discuss the latest information on creating and programming larger than 4 port SpaceWire routers using this ASIC. The paper will describe the SpaceWire ASIC Evaluation Board that has been created for prototype development using the ASIC in a COTS chassis. Finally the paper will describe the integration of the SpaceWire core and other functional upgrades that were included in the Golden Gate ASIC, our latest bridge ASIC fabricated for standalone or processor bridge use in Spacecraft processing.

1. SPACEWIRE ASIC FEATURES REVIEW

The BAE Systems SpaceWire arose from a joint development between BAE Systems and NASA Goddard Space Flight Center (GSFC) merging the SpaceWire IP from GSFC into the Processor Bridge family from BAE Systems [1]. A block diagram of the SpaceWire ASIC is shown in Figure 1. The ASIC contains four SpaceWire ports, each of which may operate up to 264 MHz through integrated LVDS interfaces, and a

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7 port router between those four ports along with two external data interface ports and a router maintenance port. The external ports connect into an on-chip bus (shown as the blue bar at the left side of Figure 1) that provides a cross-bar switch between the various cores attached to it. Thus SpaceWire sourced or destined data may be connected to one of two 32 bit 33 MHz PCI 2.2 compliant busses, a 2 GB memory space for external memory, 32 KB of internal SRAM, a DMA controller and an embedded microcontroller[3] that may be used to manage or direct the ASIC traffic. Slower speed connections may be made with discrete I/O, a UART interface, a JTAG Interface as well as several clocks and timing circuits.

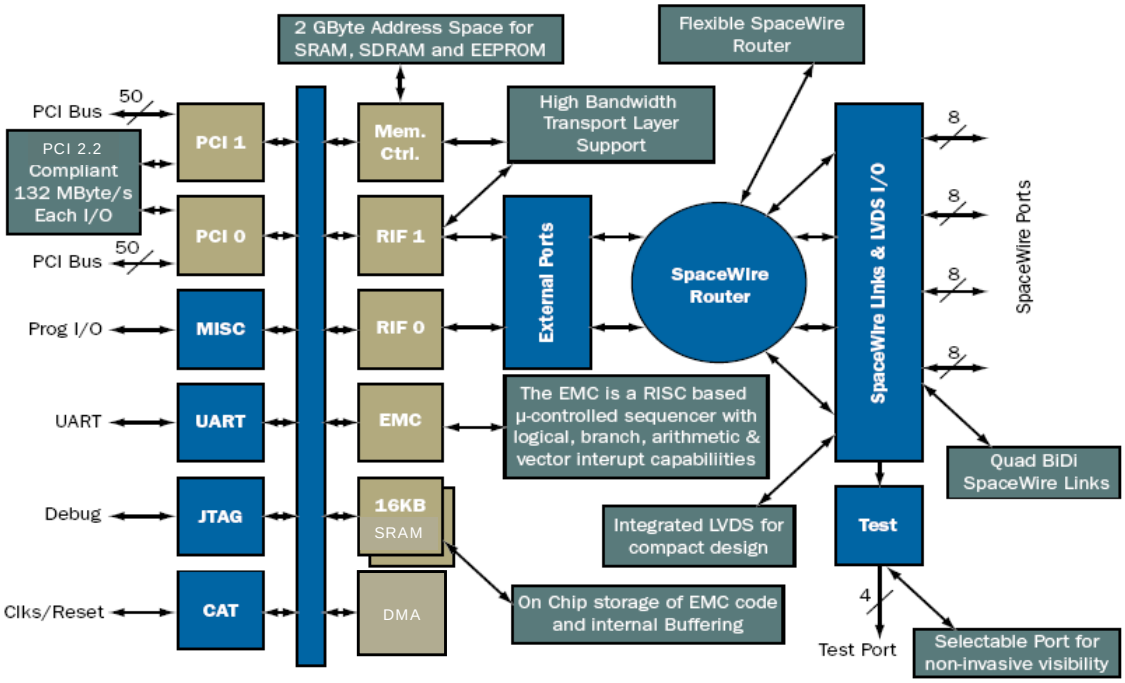


Figure 1. SpaceWire ASIC Block Diagram

The SpaceWire ASIC operates over the full military temperature range and is powered by 2.5V supply for its core and 3.3V supply for its I/O. It is packaged in a 625 pin Column Grid Array package. It is rated for operation over 200 Krad (Si) total ionizing dose, while experiencing single event upsets under 10^{-9} upsets / bit-day. Thus the SpaceWire ASIC is a complete bridging system on a single chip and is being applied to several spacecraft applications including the Geostationary Operational Environmental Satellite (GOES-R) and the NASA Lunar Reconnaissance Orbiter (LRO).

2. SpaceWire Use within LRO

The LRO is a satellite designed to map the terrain in intimate detail and will launch in early 2009. SpaceWire was selected as the main data interface throughout the spacecraft [2] and is visible in the spacecraft functional block diagram shown in Figure 2. Note the SpaceWire links connecting the RAD750 SBC to the HK/IO, Ka-Comm and S-Comm units as well as the link from the HK/IO to the Mini-RF Payload.

The RAD750 SBC was described in detail in [2]. We will now discuss the use of the SpaceWire ASIC within the Mini-RF payload.

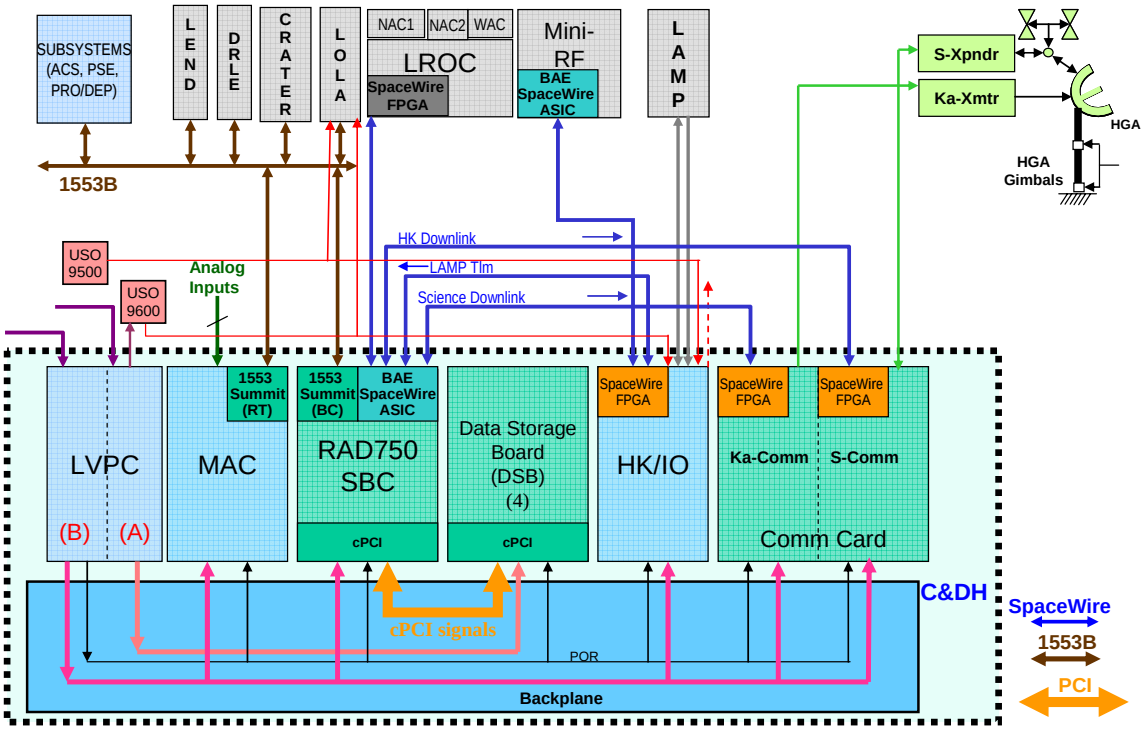
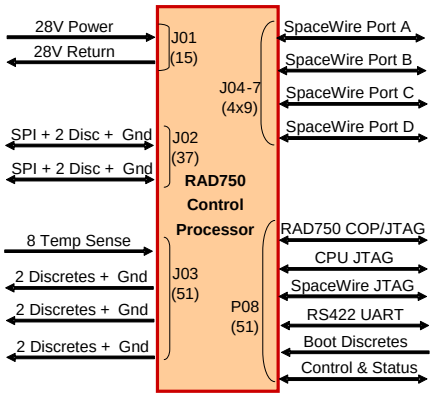


Figure 2. LRO C&DH Architecture

3. MINI-RF PROCESSOR SLICE

The Mini-RF Payload is a radar system used to search for ice in the craters at the poles of the moon. Controlling the Mini-RF Payload is a RAD750 Control Processor Slice. Processor connections to the Control Processor Slice of the Mini-RF Payload are shown in Figure 3. The Control Processor provides the direct link to the Bus Electronics via the HK/IO module and receives commands and reports status over that interface to the RAD750 SBC. The Control Processor manages the Mini-RF payload and uses SpaceWire links to control high performance elements in the payload. High speed data is also routed back to the HK/IO unit for storage and transmission to earth. Slower speed interfaces (Serial Peripheral Interconnect or SPI) are used for controlling the lower performance functions in the payload. A block diagram of the processor I/O is shown below. Connector designations and pin counts are shown.



The Mini-RF RAD750 Control Processor Slice is a self-contained enclosed single board computer that runs directly off of spacecraft 28V power. A block diagram of the Control Processor is shown in Figure 4. Colors are used to show voltage regions. Power is converted and filtered from 28V down to +12, +5V and +3.3V. The 3.3V is further regulated to 2.5V

for use by the various devices needing that core voltage. The design of the power conversion for the Control Processor Slice was especially challenging. Initially we selected some promising COTS converters and point of load devices. Radiation testing of these devices uncovered single event latch-up problems which disqualified their usage. A set of less efficient but radiation hardened devices were then selected.

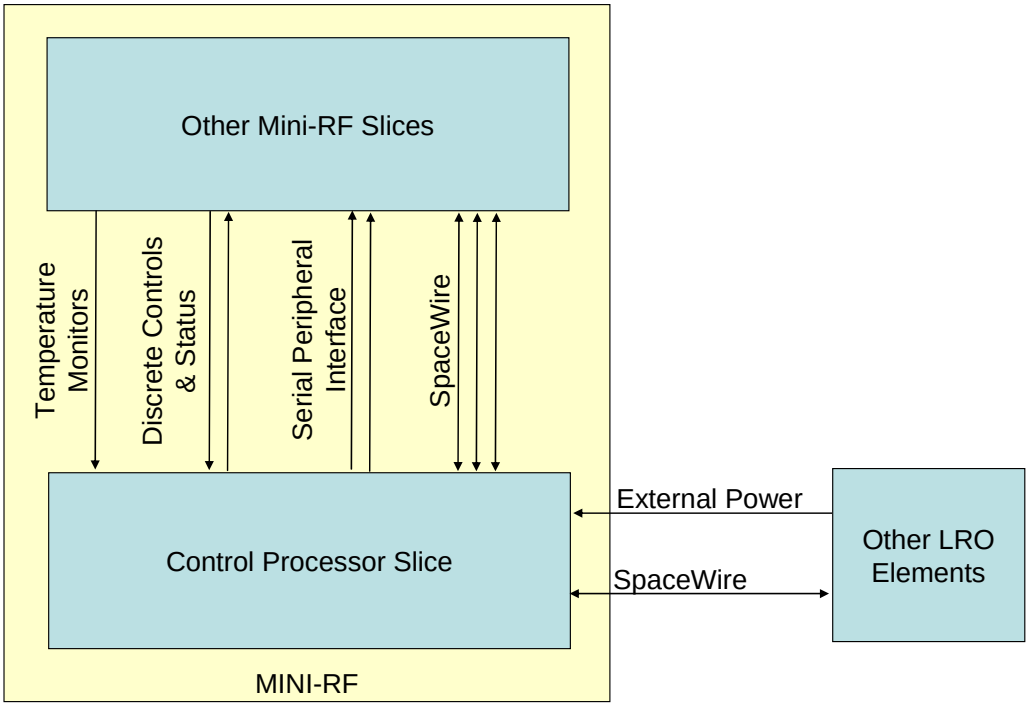


Figure 3. Mini-RF Processor Interconnect Block Diagram

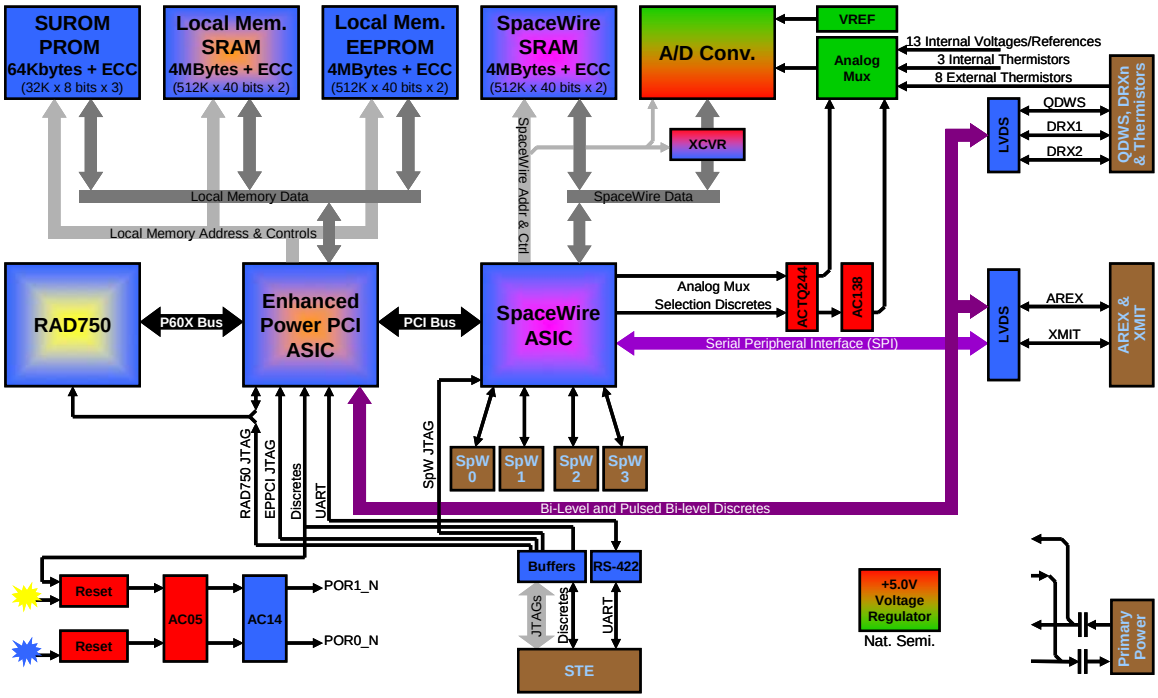


Figure 4. Mini-RF RAD750 Control Processor Block Diagram

At the left center of Figure 4 is the RAD750 Processor running at 132 MHz[5]. This is connected to a processor bridge chip that interfaces to the Processor's onboard memory and to the SpaceWire ASIC. 64KB of PROM, 4 MB of EEPROM and 4 MB

of SRAM provide a full array of memory for the controller software to manage the Mini-RF payload. The Enhanced Power PCI ASIC also provides connections to the boards software test interfaces, a UART and JTAG as well as various configuration discretes. The SpaceWire ASIC provides its four routed SpaceWire ports for external control and data movement. It also utilized the EMC in the ASIC to run a software controlled SPI interface to the slower elements of the payload. The SpaceWire ASIC's memory interface is used to provide 4 MB of SRAM for message buffering and for spare storage that the RAD750 may utilize. This interface was also used to connect an Analog to Digital Converter to several voltage measuring circuits and Thermistors. Thus, the Mini-RF RAD750 Controller took full advantage of the SpaceWire ASIC's many interfaces and capabilities to avoid the need for the typical glue logic FPGA so common on most processing and interface applications. By using all off the shelf components, this card was able to be developed, brought up and integrated quicker than if it had included an FPGA design.

The RAD750 Controller Printed Wiring Board was mounted in a standalone slice with all connectors brought to D and D sub miniature cables. Thus there were no bus interfaces; however, SpaceWire was a natural for its point to point connections with other spacecraft busses. 3D representations of the design are shown in Figure 5. The SpaceWire connectors are on the top of the right drawing. Note the tabs that were used to join the slice to the deck or slice below it and the slice above it. Getting these to be accessible for mounting while also being able to connect the many cables was a particularly challenging problem.

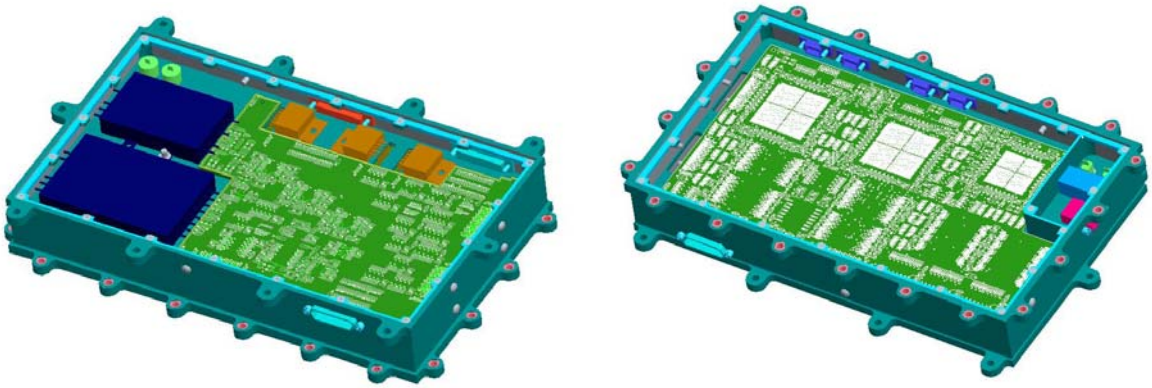
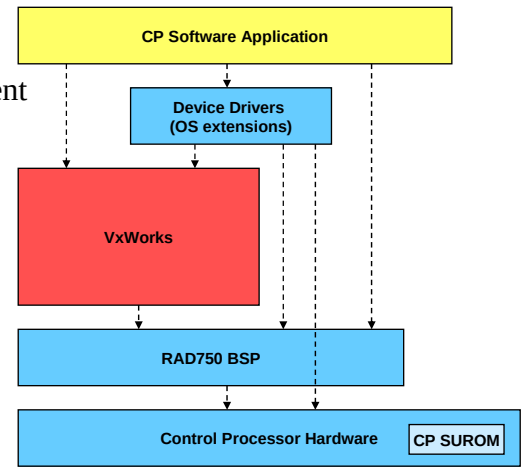


Figure 5. Controller Slice Isometric Physical Views with Covers Removed – Top and Bottom

4. MINI-RF PROCESSOR SOFTWARE

The RAD750 Controller relies on PROM-stored resident software for booting and EEPROM-stored resident software for the Operational Code and its operating system support. The internal structure of the software support layers is shown in the diagram to the right. SUROM is resident in the PROM on Controller Slice. Wind River's VXWorks is used as the real time operating system supported by board support and device driver extensions for this particular design. The Mini-RF Software Application



calls various routines from these in order to access the underlying hardware including extensions to use all the functions attached to the SpaceWire ASIC. Software routines were created and made part of the support software in order to sample telemetry and to send SPI messages to the other slices in the system as well as access any discrete signals from other modules. The combined code module was stored in the EEPROM on Control Processor Slice.

The Mini-RF Control Processor was designed to use off the shelf components and not stress the interfaces or processor. Because of board clock selections, the SpaceWire links may be configured up to 200 MHz each on this design but only were required to provide data at 40 MHz for the LRO mission. The Control Processor has been built, qualified, tested and integrated into the Mini-RF Payload, part of the 2009 LRO mission.

5. SPACEWIRE EVALUATION BOARD

The 6U-220 LRO SBC [2] is one of the most complex RAD750 single board computers built to date. A subset of this design was mapped onto a smaller 6U-160 board to make the SpaceWire ASIC available for prototyping usage in COTS CompactPCI backplanes. A block diagram of the evaluation board is shown in Figure 6. Note that there is no separate processor on this card; however the embedded microcontroller (EMC) in the SpaceWire ASIC may be utilized as a card controller and 256KB of ECC-protected EEPROM is provided to store EMC code and variables. 4 MB of SRAM is provided to store messages or as a buffer for the EMC.

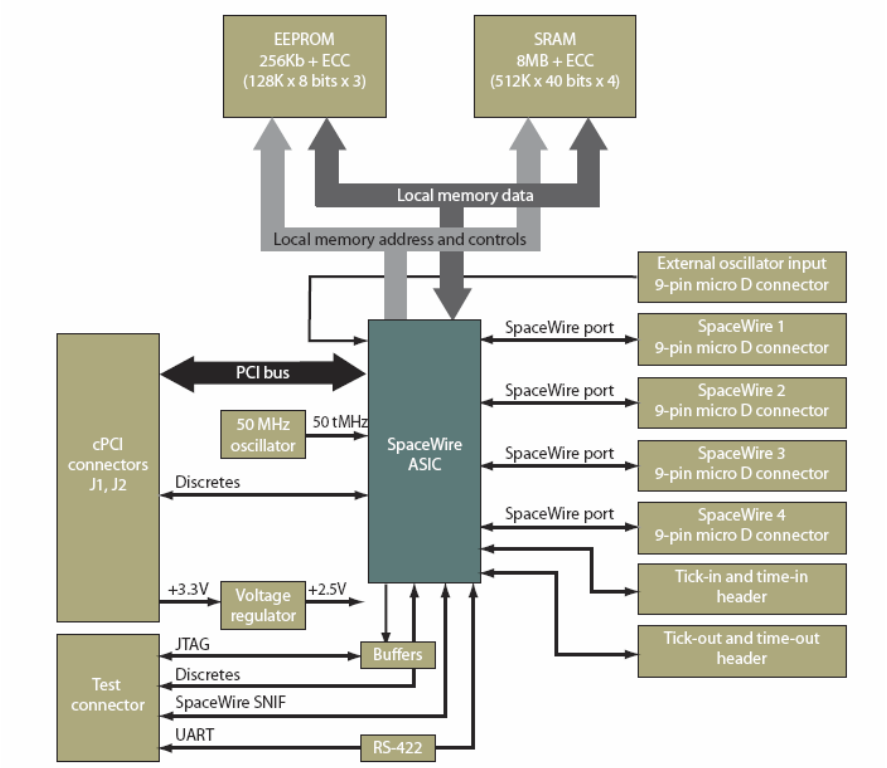


Figure 6. SpaceWire Evaluation Board Block Diagram

The SpaceWire Evaluation board has four SpaceWire ports and the integrated router and a 33 MHz 32 bit PCI 2.2 Bus interface for connecting to other boards as well as UART and JTAG test interfaces. The board runs solely off of a 3.3V supply.

The board has been built and tested with COTS SpaceWire test equipment. Two photos of the tested evaluation board is shown in . From a component point of view, this could fit on a 3U card; however the engineering required to incorporate all the front panel connectors in the small space was prohibitive for an evaluation card.

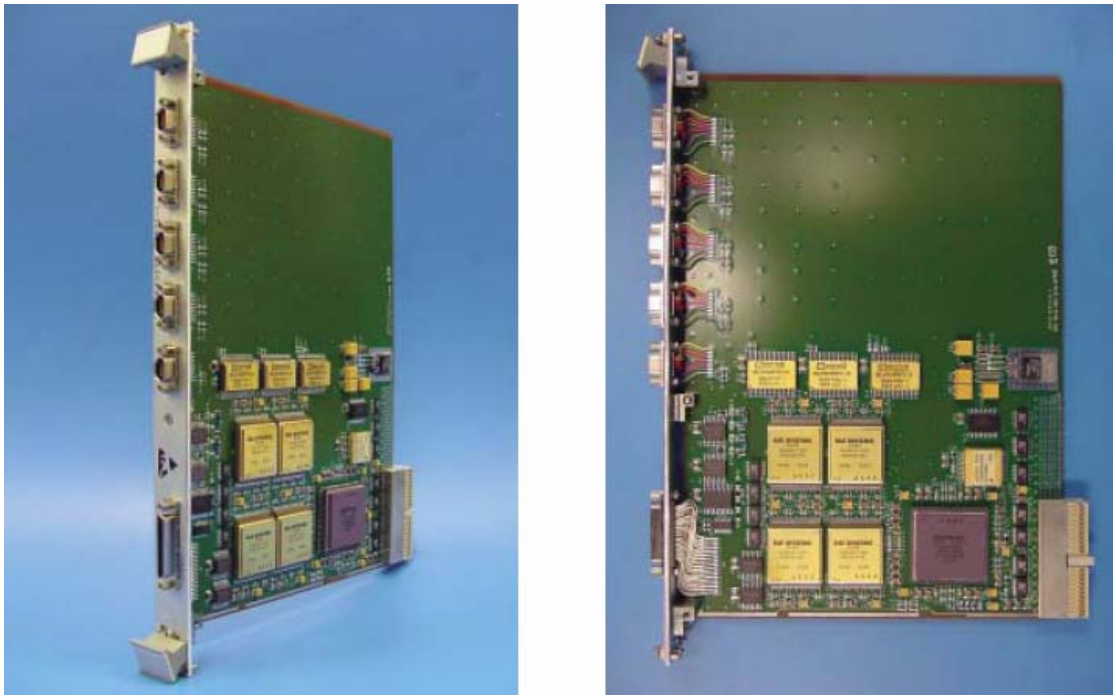


Figure 7. SpaceWire ASIC Evaluation Board Photos

6. MULTI-PORT ROUTERS

The SpaceWire ASIC Evaluation Boards may be grouped together on a CompactPCI backplane to create six or more ports of a multi-port router [1] as shown in . These could either be controlled by one of the embedded EMCs[3] or some other COTS processing card, such as the BAE RAD750 Commercial Evaluation card, could be used. The primary connection between the boards is the PCI Bus. Packets arriving on one SpaceWire ASIC may be mapped off the ASIC to the PCI Bus and then sent to the proper addressed other SpaceWire ASIC where the packet may be recreated as sent out on another SpaceWire Port. Analysis of these interfaces show that the 33 MHz 32 bit PCI bus has sufficient bandwidth (1056 Mbps) to handle small numbers of simultaneous high speed packets (100 to 250 Mbps) or larger numbers of lower speed packets (under 100 Mbps). If after analyzing the traffic more simultaneous switching bandwidth is needed, one or two of the SpaceWire ports on each ASIC may be connected to others so that some or the highest priority high speed packets would not be required to leave the SpaceWire fabric. For example, a group of four SpaceWire evaluation boards could provide anywhere from an 8 to 16 port router depending the bandwidth of the using nodes.

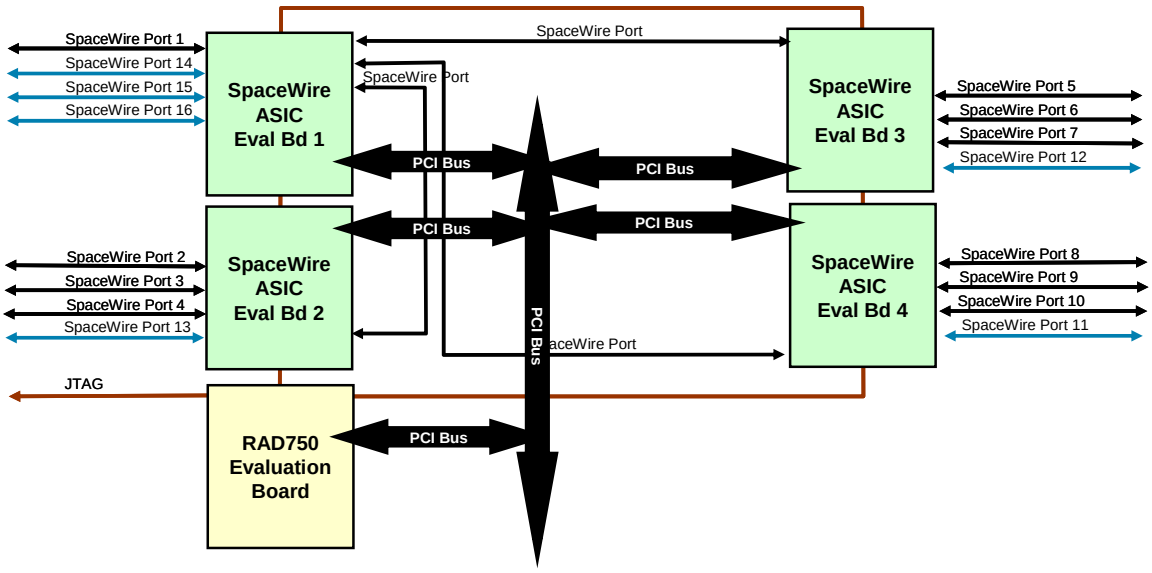


Figure 8. Multi-Port Router Using SpaceWire ASIC Evaluation Boards

7. GOLDEN GATE ASIC

BAE is fabricating its latest bridge ASIC, the Golden Gate ASIC. This device marries three of the most important interface devices onto a single radiation-hardened silicon ASIC, namely the Enhanced Power PCI Processor Bridge, the SpaceWire Bridge and 1553 Interface Bridge. It expands the size and speed of the PCI interfaces and provides a generic FIFO interface. Additionally, the EMC, DMA, discretes, internal memory and clocks are upgraded. A block diagram of the Golden Gate ASIC is shown in Figure 9.

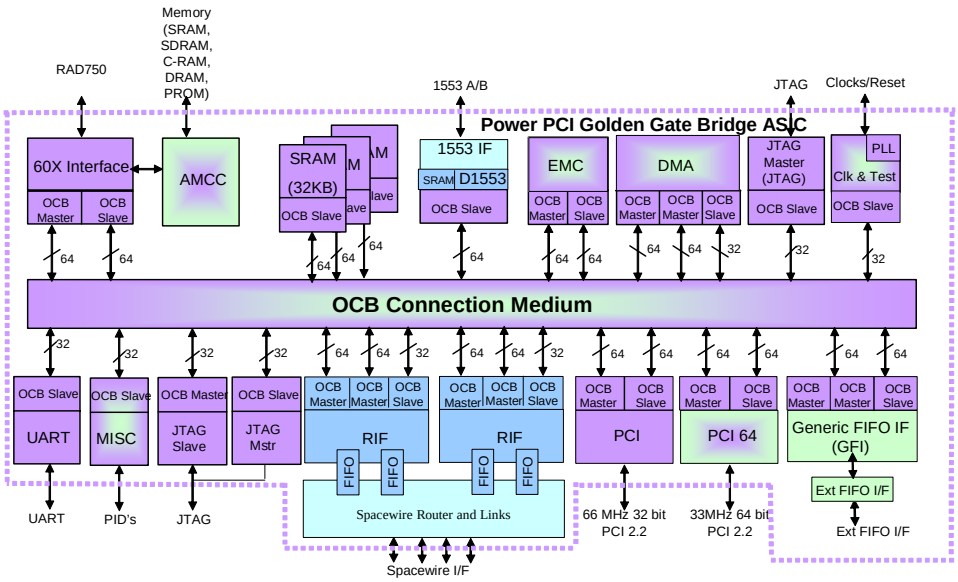


Figure 9. Golden Gate ASIC Block Diagram. Purple blocks represent reused cores.

This device utilizes an updated version of the NASA GSFC SpaceWire IP and a COTS 1553 interface IP core integrated into the On-Chip Bus. This device will result in significant savings in board area, power and higher performance processing when used on future processing applications.

8. SUMMARY

The BAE Systems SpaceWire ASIC has now been used in several space applications and will be a principal interface device in the upcoming NASA LRO Mission for command and data handling and payload control applications. Many of its system-on-a-chip capabilities were utilized on the Mini-RF Control Processor resulting in a small efficient slice that may find use in future systems. BAE has captured the essence of the LRO and Mini-RF Single board computers and distilled them into a SpaceWire Evaluation board for lab prototyping of 4 port or larger router configurations. The new Golden Gate ASIC will provide up to a 3x savings in real estate, improved power and performance and an updated SpaceWire interface. This along with the RAD6000 Microcontroller [4] mentioned at last year's conference provide application users two different single chip solutions marrying SpaceWire with processing applications spanning small instruments to multi-processor payloads.

9. REFERENCES

[1] Marshall, Joseph R. & Berger, Richard W., "A One Chip Hardened Solution for High Speed SpaceWire System Implementations", *2007 International SpaceWire Conference*, Dundee, Scotland, September 2007.

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[3] Marshall, Joseph R. & Robertson, Jeffrey, "An Embedded Microcontroller for Spacecraft Applications", *IEEE Aerospace Conference 2006 Proceedings*, Big Sky, Montana, March 2006.

[4] Berger, Richard W. et. al., "A System-On-Chip Radiation Hardened Microcontroller ASIC With Embedded SpaceWire Router", *2007 International SpaceWire Conference*, Dundee, Scotland, September 2007.

[5] Richard W. Berger et. al., "The RAD750 - A Radiation Hardened PowerPC Processor for High Performance Spaceborne Applications", *IEEE Aerospace Conference 2001*, April 2001.